REMARKS

Claims 1, 2, 4, 7-9, 11-15, 17, 18, and 22-28 are all the claims pending in the application. Claims 1, 7, and 15 are independent. This Amendment amends claims 1, 7, 9, 15, and 18 adds claim 25-28, and addresses each point of rejection raised by the Examiner. Favorable reconsideration is respectfully requested.

Applicants thank the Examiner for the indication that claims 12, 23, and 24 would be allowed if rewritten in independent form. Applicants ask that the rewriting of these claims be held in abeyance until the Examiner has had an opportunity to reconsider the independent claims in view of the remarks and amendments provided herein.

Claims 1-2, 4, 7-9, 11, 13-15, 17-18, and 22 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,420,992 to Killian *et al.* ("Killian").

At least two features distinguish the claimed invention from Killian.

First, Killian does not selectively zero-extend and sign-extend a truncated address.

While Killian does disclose extension circuitry that can selectively use either zero or sign extension such as extension circuit 120 in FIG. 4A (*see* Killian col. 15, line 54 to col. 16, line 3), such extension circuitry is used for data, rather than extending truncated addresses.

Referring to FIG. 5D, Killian does take one-half of the address bits (VA (63..32)) and feed them into a multiplexer 172, which the Examiner cites as truncation. And as noted by the Examiner, if the device is in "32-user mode," the multiplexer 172 substitutes zeros for these higher order bit (*i.e.,* zero-extending). *See* Killian col. 18, lines 13-15 and col. 19, lines 64-68. However, while this may constitute zero-extension of VA(31..0), there is no sign-extension of this truncated address. It is "assumed" that any 32-bit mode address presented to the address translation mechanism is in sign-extended form (*see* Killian col. 18, lines 11-17), such that there is no sign-extension of the truncated address bits in 32-bit kernel mode.

Second, Killian does not disclose an unsigned address space subset of the first bit size. In 32-bit mode, the addresses are still stored and manipulated as 64-bit sign-extended entities. *See* Killian col. 17, lines 29-31. Applicants understand the Examiner's position to be that the user virtual address space, as illustrated in FIG. 3A of Killian, constitutes an unsigned address space, since VA(31)=0 for the 32-bit user mode addresses. Even so, this is not an address space of the

first bit size, but an address space of the first bit size minus one. For example, whereas in Killian a 32-bit instruction in 32-bit user mode can address 0-2 GB and in 32-bit kernel mode can address -2 GB to +2GB, in a 32-bit application ported to a 64-bit environment embodiment of the present invention, the 32-bit application can operate within an unsigned 0 to 4 GB, and within signed -2 GB to +2 GB. *See, e.g.,* page 2, line 23 to page 3, line 2. Applicants have amended claims 1, 7, and 15 to emphasize this point.

Further, with regard to claim 11, generation of an address exception in Killian is an absolute based on whether bit VA(31) is one, which equals overflow. *See, e.g.,* Killian col. 16, lines 51-60. There is no comparison of the generated reference with the extended, truncated generated address reference, as recited in the claim.

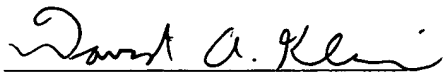
Reconsideration is requested.

Applicants authorize the Commissioner to charge any fees determined to be due with the exception of the issue fee and to credit any overpayment to Deposit Account No. 11-0600.

The Examiner is invited to contact the undersigned at (202) 220-4209 to discuss any matter concerning this application.

Respectfully submitted,
KENYON & KENYON

Dated: August 29, 2005



David A. Klein
Reg. No. 46,835

Kenyon & Kenyon
1500 K Street, N.W.
Suite 700
Washington, D.C. 20005
Tel: (202) 220-4200
Fax: (202) 220-4201

577720_1.DOC